WHAT IS CLAIMED IS:

1. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire including a plurality of gate lines and a plurality of gate pads connected to the gate lines on a substrate having a display area and a peripheral area, the gate lines located substantially in the display area and the gate pads located substantially in the peripheral area;

forming a gate insulating layer pattern that covers portions of the gate wire and the substrate in the display area and exposes at least a part of each gate pad;

forming a semiconductor pattern on the gate insulating layer pattern;

forming an ohmic contact layer pattern on the semiconductor pattern;

forming a data wire including a plurality of data lines, source electrodes connected to the data lines and drain electrodes located substantially in the display area and a plurality of data pads located substantially in the peripheral area on the ohmic contact layer pattern;

forming a passivation layer pattern; and

forming a plurality of pixel electrodes connected to the drain electrodes,

wherein the gate insulating layer pattern is formed along with at least one of the semiconductor pattern, the ohmic contact layer pattern, the data wire, the passivation layer pattern and the pixel electrodes through a single photolithography process using a photoresist pattern having a thickness that varies depending on positions.

2. The method of claim 1, wherein the photoresist pattern has a first portion located over the gate pads, a second portion that is thicker than the first portion and located in the display area, and a third portion that is thicker than the second portion.

3. The method of claim 2, wherein

the photoresist pattern is formed on the passivation layer;

the gate insulating layer pattern is formed along with the semiconductor layer pattern and the passivation layer pattern; and

the step of forming the gate insulating layer pattern, the semiconductor layer pattern and the passivation layer pattern is comprising the steps of:

forming a gate insulating layer;

forming a semiconductor layer on the gate insulating layer;

forming a passivation layer over the semiconductor layer;

etching the passivation layer and the semiconductor layer under the first portion of the photoresist pattern, and the second portion of the photoresist pattern at a time;

removing the second portion of the photoresist pattern to expose the passivation layer thereunder by an ashing process;

etching the gate insulating layer and the passivation layer by using the photoresist pattern as an etch mask to expose the gate pads under the first portion of the photoresist pattern and to expose the semiconductor layer under the second portion of the photoresist pattern; and

removing a portion of the semiconductor layer under the second portion by using the photoresist pattern as an etch mask.

4. The method of claim 3, wherein the data pads are exposed in the step of etching the portions of the passivation layer and the semiconductor layer.

5. The method of claim 3, wherein the data pads are exposed in the step of etching the passivation layer and the gate insulating layer.

6. The method of claim 3, wherein the drain electrodes are exposed in the step of etching the passivation layer.

7. The method of claim 3, wherein the drain electrodes are exposed in the step of etching the portions of the passivation layer and the semiconductor layer.

8. The method of claim 3, wherein the step of etching the passivation layer and the semiconductor layer is performed by dry etch using SF_6+O_2 or SF_6+HCl as an etch gas mixture.

9. The method of claim 3, wherein the ashing process is performed by using N_2+O_2 or O_2+Ar gas mixture.

10. The method of claim 3, wherein the semiconductor layer is made of amorphous silicon, and the step of etching the passivation layer is performed by using one selected from the group consisting of SF_6+O_2, SF_6+N_2, CF_4+O_2 and $CF_4+CHF_3+O_2$.

11. The method of claim 3, wherein the step of removing the semiconductor layer is performed by dry etch using Cl_2+O_2 or $SF_6+HCl+Ar+O_2$ as an etch gas mixture.

12. The method of claim 1, wherein a plurality of redundant gate pads and redundant data pads respectively covering the gate pad and the data pad are formed in the step of forming the pixel electrode.

13. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire including a plurality of gate lines, gate electrodes and gate pads;

forming a gate insulating layer pattern that covers the gate wire except for at least a part of the gate pads;

forming a semiconductor pattern on the gate insulating layer pattern;

forming an ohmic contact layer pattern on the semiconductor pattern;

forming a data wire including a plurality of data lines, source electrodes, drain electrodes and data pads on the ohmic contact layer pattern;

forming a passivation layer pattern; and

forming a plurality of pixel electrodes connected to the drain electrodes,

wherein the gate insulating layer pattern is formed along with at least one of the semiconductor pattern, the ohmic contact layer pattern, the data wire, the passivation layer pattern and the pixel electrode through a photolithography process, and the photolithography process is comprising the steps of:

coating a photoresist layer;

exposing the photoresist layer through a photomask having a first part, a second part and a third part having a transmittance different from one another; and

developing the photoresist layer to form a photoresist pattern.

14. The method of claim 13, wherein the transmittance of the second part of the photomask is 20 % to 60 % of that of the first part and the transmittance of the third part is lower than 3 % of that of the first part.

15. The method of claim 13, wherein the photomask has a mask substrate and at least one mask layer, and the difference of transmittance between the first part and the second part is obtained by adjusting the mask layer of the first part and the second part of materials.

16. The method of claim 13, wherein the photomask has a mask substrate and at least one mask layer, and the difference of transmittance between the first part and the second part is obtained by differentiating the thickness of the mask layer.

17. The method of claim 13, wherein the photomask has a mask substrate and at least one mask layer, and the difference of transmittance between the first part and the second part is obtained by forming slits or a grid pattern smaller than the resolution of the stepper in the mask layer.

18. A manufacturing method of a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire including a plurality of gate lines, gate electrodes and gate pads;

forming a gate insulating layer pattern that covers the gate wire and exposes at least a part of the gate pad;

forming a semiconductor pattern on the gate insulating layer pattern;

forming an ohmic contact layer pattern on the semiconductor pattern;

forming a data wire including a plurality of data lines, source electrodes, drain electrodes and data pads on the ohmic contact layer pattern;

forming a passivation layer pattern; and

forming a plurality of pixel electrodes connected to the drain electrodes,

wherein the gate insulating layer pattern is formed along with at least one of the semiconductor pattern, the ohmic contact layer pattern, the data wire, the passivation layer pattern and the pixel electrode through a photolithography process, and the photolithography process is comprising the steps of:

coating a photoresist layer;

exposing the photoresist layer through a first photomask having a first part and a second part having a transmittance higher than the first part, and a second photomask having a third part having a transmittance higher than the first part and lower than the second part; and

developing the photoresist layer to form a photoresist pattern.

19. The method of claim 18, wherein the transmittance of the third part of the photomask is 20 % to 60 % of the transmittance of the second part.

20. The method of claim 18, wherein the first photomask and the second photomask respectively have a mask substrate and at least one mask layer, and the difference of transmittance between the second part and the third part is obtained by making the mask layer of the first photomask and the second photomask have different transmittance.

21. The method of claim 18, wherein the first photomask and the second photomask respectively have a mask substrate and at least a mask

layer, and the difference of transmittance between the second part and the third part is obtained by differentiating the thickness of the mask layer.

22. A photolithography method of thin films, comprising the steps of:

forming at least one layer of thin film on a substrate;

coating a photoresist layer on the thin film;

exposing the photoresist layer to light through at least one photomask having more than three parts having transmittance different from one another;

developing the photoresist layer to form a photoresist pattern having a varying thickness according to locations; and

etching the thin film along with the photoresist pattern.

23. The method of claim 22, wherein the etching step uses a dry etch.

24. The method of claim 22, wherein the photoresist layer is made of a positive photoresist.

25. A method for fabricating thin films by photolithography, comprising the steps of:

forming as least one layer of thin film on a substrate;

forming on the thin film a photoresist pattern that has a first portion, a second portion having a thickness thicker than the first portion and a third portion of which thickness is thicker than that of the second portion;

etching the thin film under the first portion of the photoresist pattern, while the second portion and the third portion of the photoresist pattern protecting the thin film thereunder;

removing the second portion of the photoresist pattern to expose the thin film thereunder, the third portion of the photoresist pattern remaining in a thickness; and

etching the exposed portion of the thin film, while the third portion of the photoresist pattern protecting the thin film thereunder.

26. The method of claim25, wherein the step of removing the second portion of the photoresist pattern is performed by an ashing process.

27. A method for a thin film transistor array panel for a liquid crystal display, comprising the steps of:

forming a gate wire including a plurality of gate lines, gate electrodes and gate pads on an insulating substrate;

depositing a gate insulating layer, a semiconductor layer, an ohmic contact layer and a conductor layer on the gate wire in sequence;

patterning the conductor layer and the ohmic contact layer by photolithography to form a data wire including a plurality of data lines, source electrodes, drain electrodes and data pads, and an ohmic contact layer pattern under the data wire;

depositing a passivation layer;

coating a photoresist layer on the passivation layer;

forming a photoresist pattern having a thickness that varies according to location by exposure and development;

etching the passivation layer, the semiconductor layer and the gate insulating layer along with the photoresist pattern to form a passivation layer pattern, a semiconductor layer pattern, and a gate insulating layer pattern

having contact holes exposing the gate pads and *a non-zero thickness* in the display area; and

forming a plurality of pixel electrodes respectively connected to the drain electrodes on the passivation layer.

28. The method of claim27, wherein a plurality of redundant gate pads and redundant data pads respectively covering the gate pads and the data pads are formed in the step of forming the pixel electrodes.

29. A method for manufacturing a thin film transistor array panel, comprising the steps of:

depositing a first metal layer on a substrate;

forming a gate wire including a plurality of gate lines and gate pads by a first photolithography process;

depositing a first insulating layer, a semiconductor layer, an ohmic contact layer and a second metal layer on the gate wire;

patterning the second metal layer and the ohmic contact layer to form a data wire including a plurality of data lines, data pads, source electrodes and drain electrodes, by a second photolithography process;

depositing a second insulating layer;

patterning the second insulating layer, the semiconductor layer and the first insulating layer to form a passivation layer pattern that covers the gate wire, the data wire and the portions of the semiconductor layer between the source electrode and the drain electrode and exposes a portion of the drain electrodes and the data pads, a semiconductor layer pattern having a separated portion at

least on the gate wire, and a gate insulating layer pattern exposing the gate pad by a third photolithography process;

depositing a transparent conductor layer; and

patterning the transparent conductor layer to form a plurality of pixel electrodes connected to the drain electrode, redundant gate pads and redundant data pads respectively covering the gate pads and the data pads.

30. The method of claim29, wherein the third photolithography process comprises the steps of:

coating a photoresist layer on the second insulating layer; and

exposing the photoresist layer by using a photomask having at least two portions of which transmittance are different from each other.

31. The method of claim 30, wherein the third photolithography process comprises a development step after the exposure to form a photoresist pattern having at least three different heights.

32. The method of claim31, wherein the third photolithography process comprises an etching step of the photoresist pattern, the second insulating layer, the semiconductor layer and the first insulating layer to remove a first portion that is the lowest portion, and the second insulating layer, the semiconductor layer and the first insulating layer thereunder to expose the gate pads, and to remove a second portion which is higher than the first portion, and the second insulating layer and the semiconductor layer thereunder, but not remove the second insulating layer under a third portion which is higher than the second portion.

33. The method of claim32, wherein the etching step of the photoresist pattern, the second insulating layer, the semiconductor layer and the first insulating layer comprises the steps of:

etching the second insulating layer, the semiconductor layer and the first insulating layer under the first portion of the photoresist pattern by using the second and the third portion as an etch stopper;

removing the second portion of the photoresist layer to expose the second insulating layer thereunder by an ashing process; and

etching the exposed portion of the second insulating layer and the semiconductor layer thereunder by using the third portion of the photoresist layer as an etch stopper.

34. The method of claim 33, wherein the ashing process is performed by using oxygen.

35. The method of claim 30, wherein the transmittance difference of the photomask is controlled by differentiating the thickness of a mask layer.

36. The method of claim30, wherein the photomask is classified into a first mask for the gate pad and a second mask for the elsewhere and the transmittance of the first mask is different from that of the second mask.

37. The method of claim29, wherein the pixel electrodes are formed just on the first insulating layer extended from under the data wire.

38. The method of claim29, wherein the semiconductor layer is made of amorphous silicon.

39. The method of claim38, wherein the ohmic contact layer is made of amorphous silicon doped with phosphorus.

40. The method of claim39, wherein the transparent conductor layer is made of indium-tin-oxide.

41. The method of claim 29, wherein the pixel electrodes are formed just on the first insulating layer extended from under the drain electrode.

42. A thin film transistor array panel, comprising:

an insulating substrate;

a gate wire including a plurality of gate lines, gate electrodes and gate pads and formed on the insulating substrate;

a gate insulating layer pattern having a contact hole exposing the gate pad and formed on the gate wire;

a semiconductor layer pattern formed on the gate insulating layer pattern;

an ohmic contact layer pattern formed on the semiconductor layer pattern;

a data wire formed on the ohmic contact layer pattern, having a planar shape substantially the same as that of the ohmic contact layer pattern, and including a plurality of source electrodes, data lines and data pads;

a passivation layer pattern formed on the data wire, having contact holes exposing the gate pad, the data pad and the drain electrode, having a planar shape substantially the same as that of the semiconductor layer pattern except for the portions of the drain electrode and the data pad, having wider width than that of the data wire, and covering the boundary line of the data wire;

an electrode pattern electrically connected to the exposed gate pad, data pad and drain electrode.

43. The thin film transistor array panel of claim 42, wherein at least a portion of the electrode pattern electrically connected to the drain electrode is in direct contact with the gate insulating layer pattern extending from under the drain electrode.

44. The thin film transistor array panel of claim 43, further comprising a storage electrode formed over the gate line, wherein the semiconductor layer pattern and the ohmic contact layer pattern have a portion interposed between the storage electrode and the gate line, and the storage electrode is connected to the electrode layer pattern.

45. The thin film transistor array panel of claim 42, wherein the shape of the gate insulating layer pattern is different from that of the passivation layer pattern under the electrode pattern.